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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,360	04/20/2004	Richard Carl Phelps	0120-030	2608
42015	7590	02/09/2006	EXAMINER	
POTOMAC PATENT GROUP, PLLC			CLEARY, THOMAS J	
P. O. BOX 270			ART UNIT	
FREDERICKSBURG, VA 22404			PAPER NUMBER	

2111

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/827,360

Applicant(s)

PHELPS ET AL.

Examiner

Thomas J. Cleary

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

2. Claims 2 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

3. In reference to Claims 2 and 3, it is unclear if the length of the bus portion refers to the physical length (the distance between the bus connection units) or the temporal length (the amount of time or number of clock cycles it takes for data to traverse the bus segment).

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 3, 5, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent Number JP 08147163 to Takemoto ("Takemoto").

6. In reference to Claim 1, Takemoto discloses an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Figure 1); a plurality of modules connected to the bus architecture (See Figure 1 Numbers 15, 17, and 19); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 1 Numbers 16, 18, and 20); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit (See Figure 1), wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units (See Figure 1 Numbers 16, 18, and 20); and each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Figure 1 Numbers 16, 18, and 20).

7. In reference to Claim 2, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses that each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the length of the bus portions concerned (See 'Purpose' in English Language Abstract).

8. In reference to Claim 3, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses that the bus portions are all equal in length (See Figure 1).

9. In reference to Claim 5, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Figure 1 Number 21).

10. In reference to Claim 12, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses a computer system comprising the apparatus (See Figure 1).

11. Claims 1, 2, 3, 5, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,325,495 to McLellan ("McLellan").

12. In reference to Claim 1, McLellan discloses an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Figure 1); a plurality of modules connected to the bus architecture (See Figure 1 Numbers 16 and 16'); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 1 Numbers 18 and 18'); and a plurality of bus portions arranged in series, each bus portion, except the

last in the series, being connected to the next portion in the series by way of a bus connection unit (See Figure 1 'Q-Stage' and 'Pipeline Stage 4'), wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units (See Figure 1 Numbers 18 and 18'); and each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Figure 1 Numbers 18 and 18').

13. In reference to Claim 2, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses that each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the length of the bus portions concerned (See Column 4 Lines 38-44).

14. In reference to Claim 3, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses that the bus portions are all equal in length (See Figure 1).

15. In reference to Claim 5, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Figure 1 Number 20).

16. In reference to Claim 12, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses a computer system comprising the apparatus (See Figure 1).

17. Claims 1, 2, 3, 5, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,555,384 to Roberts et al. ("Roberts").

18. In reference to Claim 1, Roberts discloses an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Figure 6); a plurality of modules connected to the bus architecture (See Figure 6 'Execution Unit(s) and Numbers 33 and 35); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 6); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit (See Figure 6), wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units (See Figure 6 'Execution Unit(s) and Numbers 33 and 35); and each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Figure 6).

19. In reference to Claim 2, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses that each bus connection unit includes output circuitry

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connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the length of the bus portions concerned (See Column 5 Lines 42-49).

20. In reference to Claim 3, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses that the bus portions are all equal in length (See Figure 6).

21. In reference to Claim 5, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Figure 6 Number 50).

22. In reference to Claim 12, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses a computer system comprising the apparatus (See Figure 6).



***Claim Rejections - 35 USC § 103***

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

24. Claims 4, 6, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto as applied to Claims 1 and 5 above, and further in view of US Patent Number 5,627,976 to McFarland et al. ("McFarland").

25. In reference to Claim 4, Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach a primary bus and a secondary bus, the primary and secondary buses being interconnected by an interface. McFarland teaches a primary bus (See Figure 1 Number 20) and secondary bus (See Figure 1 Number 25) interconnected by an interface (See Figure 1 Number 45), a plurality of modules connected to the primary bus (See Figure 1 Numbers 32, 35, and 37), and a plurality of modules connected to the secondary bus (See Figure 1 Numbers 40 and 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the pipelined bus structure of Takemoto, resulting in the invention of Claim 4, because a dual bus system allows a very fast bus to interface with a much slower bus in a way that the high

bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and because pipelines with bypass stages reduce power consumption (See 'Purpose' in English Language Abstract of Takemoto).

26. In reference to Claim 6, Takemoto teaches the limitations as applied to Claim 5 above. Takemoto does not teach a primary bus and a secondary bus, the primary and secondary buses being interconnected by an interface. McFarland teaches a primary bus (See Figure 1 Number 20) and secondary bus (See Figure 1 Number 25) interconnected by an interface (See Figure 1 Number 45), a plurality of modules connected to the primary bus (See Figure 1 Numbers 32, 35, and 37), and a plurality of modules connected to the secondary bus (See Figure 1 Numbers 40 and 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the pipelined bus structure of Takemoto, resulting in the invention of Claim 6, because a dual bus system allows a very fast bus to interface with a much slower bus in a way that the high bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and because pipelines with bypass stages reduce power consumption (See 'Purpose' in English Language Abstract of Takemoto).

27. In reference to Claim 7, Takemoto and McFarland teach the limitations as applied to Claim 4 above. McFarland further teaches that the first plurality of modules are latency tolerant and the second plurality of modules are latency intolerant (See Figure 1, Column 2 Line 61 – Column 3 Line 12 and Column 5 Lines 21-32).

28. In reference to Claim 8, Takemoto and McFarland teach the limitations as applied to Claim 4 above. McFarland further teaches that the primary bus is one pipeline stage in length (See Figure 1).

29. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto as applied to Claim 1 above, and further in view of US Patent Number 5,128,926 to Perlman et al. ("Perlman").

30. In reference to Claim 9, Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach that transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated. Perlman teaches splitting a large packet into pieces which are smaller than the maximum packet size and transmitting the smaller packets separately (See Column 2 Lines 55-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Takemoto with the packet splitting of Perlman, resulting in the invention of Claim 9, in order to relieve the computation burden

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by reducing the probability of errors in transmission (See Column 2 Line 64 – Column 3 Line 14 of Perlman).

31. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto as applied to Claim 1 above, and further in view of US Patent Number 5,925,118 to Revilla et al. ("Revilla").

32. In reference to Claim 10 Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach separate read, write, and transaction buses. Revilla teaches the use of separate read (See Figure 1 Number 34), write (See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Takemoto with the split bus system of Revilla, resulting in the invention of Claim 10, in order to provide a high throughput of data between functions (See Column 2 Lines 17-31 of Revilla).

33. In reference to Claim 11 Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach that the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive system clock cycles. Revilla teaches the use of separate read (See Figure 1 Number 34), write (See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36) which have a

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width sufficient to permit read and write request transactions to alternate in successive system clock cycles (See Column 3 Lines 12-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Takemoto with the split bus system of Revilla, resulting in the invention of Claim 11, in order to provide a high throughput of data between functions (See Column 2 Lines 17-31 of Revilla).

### ***Response to Arguments***

34. Applicant's arguments, see Pages 8-13, filed 29 November 2005, with respect to the rejection(s) of claim(s) 1-12 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Takemoto, McLellan, and Roberts.

### ***Conclusion***

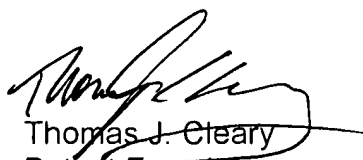
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC



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